

REMARKS

Claims 1-20 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the following remarks.

Claim Rejections - § 102

1) Claims 1, 13, and 14 stand rejected under 35 U.S.C 102(e) as being anticipated by Weaver [U.S. Patent Pub. 2004/0230933], as set forth in paragraph 2 of the Office Action.

It is respectfully submitted that Weaver does not at least teach, *"determining a structural metric through an analysis of the logic network"* and *"using the structural metric during the logical synthesis to predict wiring congestion of the circuit design model"* ... *"before assigning physical locations to the circuits"*, as essentially recited in claims 1, 13, and 14.

In the claimed inventions, a structural metric (e.g., a predictor of wiring congestion of the circuit design) is derived from data that does not include information about the physical locations of the circuits. For example, the structural metric is determined from an analysis of a logic network of an RTL before assigning physical locations of the circuit.

However, in Weaver, a routability determination is made from a placed circuit design, meaning that Weaver's determination is derived from data that includes placement information. For example, Weaver states (in para. 0034) that "[u]pon completion of step 6, placement of the cells is checked for circuit congestion, step 8 of the FIGURE."

A determination from data that includes placement information is clearly different from the claimed structural metric that is derived from data that does not include placement information.

The Examiner essentially contends (in p. 6 of the Final Office Action) that the feedback of the routability determination from step 8 to step 2 in Weaver discloses using a structural metric during logical synthesis (step 2) to predict wiring congestion (step 8).

However, consider that the routability determination in Weaver is based on data that includes placement information and that the congestion determination is based on placement data in every iteration. The Examiner's suggested interpretation of the figure of Weaver, which essentially changes a starting point in the figure, does not negate Weaver's express teaching that a congestion determination is based on placement data (see elements 6 and 8 in the figure). Therefore, Weaver can not disclose the claimed structural metric.

For at least these reasons, Weaver fails to anticipate claims 1, 13, and 14. Thus, claims 1, 13 and 14 are believed to be patentable over Weaver.

2) Claims 1-20 stand rejected under 35 U.S.C 102(e) as being anticipated by McElvain [U.S. Patent Pub. 2006/0095872], as set forth in paragraph 3 of the Office Action.

It is respectfully submitted that McElvain does not at least disclose or suggest, *“determining a structural metric through an analysis of the logic network”* and *“using the structural metric during the logical synthesis to predict wiring congestion of the circuit design model”* ... *“before assigning physical locations to the circuits”*, as essentially recited in claims 1, 13, and 14.

The Examiner contends (in p. 4 of the Final Action) that figures 23 and 35 of McElvain discloses determination of the claimed structural metric. However, the Examiner fails to state which individual step or group of steps of figures 23 or 35 are relevant.

Further, the Examiner fails to provide any explanation or cite any support from McElvain that would suggest step(s) of figures 23 or 35 disclose the claimed structural metric.

The Examiner's anticipation analysis instead primarily focuses on steps 1001, 1003, and 1005 in figure 22 of McElvain, and how each step may be repeated in iterations to satisfy design requirements and to optimize the design. In particular, the Examiner states that "it is the iterations of operations 1001-1005 in fig 22 that makes the wiring congestion prediction/consideration/analysis/detection/estimation possible during logical synthesis due to the loop/iteration."

However, it is not the iterations that are relevant, but whether McElvain discloses derivation of a metric like the claimed structural metric. As discussed above, the claimed structural metric is derived from data that does not include placement information. For example, the claimed structural metric is determined from an analysis of a logic network of an RTL before assigning physical locations of the circuit. However, the Examiner has failed to show how a similar structural metric (e.g., one that is derived from data that does not include placement information) is disclosed by McElvain. Further, the methods of figures 23 and 35 do not disclose generation of a similar structural metric, nor application of such a metric during McElvain's logical synthesis (1001) stage. Clearly, analysis and optimization (1005) occur only after placement (1003); no prediction is determined before placement, essentially as claimed.

It is further submitted that McElvain does not disclose or suggest, "*using the structural metric during a technology independent synthesis stage of the logic synthesis stage*", as recited in claim 4.

The Examiner contends (in p. 4 of the Final Office Action) that using the structural metric during a technology independent synthesis stage of logical synthesis is disclosed by figures 22 and 35 of McElvain.

However, the Examiner fails to state which individual step or group of steps of figures 22 or 35 are relevant. Further, the Examiner fails to provide any explanation or cite any support from McElvain that would suggest step(s) of figures 22 or 35 disclose using the claimed structural metric during a technology independent synthesis stage of logical synthesis.

In any event, figure 22 merely generally discloses a logical synthesis stage (1001) and not use of the claimed structural metric during a technology independent stage of the logical synthesis stage (1001). Further, figure 35 does not mention logical synthesis and paragraph [0137] of McElvain states that step 1450 of figure 35 may occur after compilation of a technology independent HDL, and step 1450 occurs during and/or after placement of the circuits.

It is further submitted that McElvain does not disclose or suggest, “the structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut (“SAPMC”), and an expansion metric”, as recited in claims 10 and 19.

The Examiner contends (in p. 4 of the Final Office Action) that the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut (“SAPMC”), and an expansion metric is disclosed by figures 26 and 28-29 of McElvain.

However, the Examiner fails to state which individual step or group of steps of figures 26, 28, or 29 are relevant. Further, the Examiner fails to provide any explanation or cite any support from McElvain that would suggest step(s) of figures 26, 28, or 29 disclose

the claimed structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric. In any event, use of a distance metric, SAPMC, or an expansion metric is not disclosed in any of the steps of figures 26, 28, or 29. In fact, use of distance metric, SAPMC, or expansion metric is not mentioned anywhere in McElvain.

For at least the foregoing reasons, McElvain fails to anticipate claims 1, 4, 10, 13, 14 and 19. Thus, claims 1, 4, 10, 13, 14, and 19 are believed to be patentable over McElvain. Moreover, claims 2-12 and claims 15-20 are believed to be patentable over McElvain at least by virtue of their respective dependencies from claims 1 and 14.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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